METHOD OF HANDLING INSTRUCTIONS WITHIN A PROCESSOR WITH DECOUPLED ARCHITECTURE, IN PARTICULAR A PROCESSOR FOR DIGITAL SIGNAL PROCESSING, AND CORRESPONDING PROCESSOR

Abstract of the Disclosure

A processing unit is associated with a first FIFO-type memory and with a second FIFO-type memory. Each instruction for loading memory stored data into a register within the processing unit is stored in the first FIFO-type memory, and other operative instructions are stored in the second FIFO-type memory. An operative instruction involving the register is removed from the second FIFO-type memory if no loading instruction which is earlier in time, and intended to modify a value of the register associated with this operative instruction is present in the first FIFO-type memory. In the presence of such an earlier loading instruction, the operative instruction is removed from the second FIFO-type memory only after the loading instruction has been removed from the first FIFO-type memory.